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EXAMINER	
CLEARY, THOMAS J	
ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 06/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,581	ADAMS ET AL.	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *41-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *41-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 41, 42, and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Number 6,513,089 to Hofmann et al. ("Hofmann"), Applicant's Admitted Prior Art ("AAPA"), US Patent Number 6,209,118 to LaBerge ("LaBerge"), US Patent Number 6,493,407 to Sheafor et al. ("Sheafor"), US Patent Number 6,173,349 to Qureshi et al. ("Qureshi"), and US Patent Number 5,469,547 to Pawlowski et al. ("Pawlowski").

3. In reference to Claim 41, Hofmann discloses a system-on-chip (SOC) semiconductor device, comprising one or more processor cores (See Figure 1 'PPC405 CPU'), one or more peripherals (See Figure 1 'I^2C', 'GPIO', and 'UART'), one or more DMA-type peripherals (See Figure 1 'DMA Controller'), and a memory subsystem (See Figure 1 'SDRAM Controller'); a first internal bus coupled to said processor cores and to said peripherals (See Figure 1 Number 101), said first internal bus carrying signals from

signal initiators to signal targets (See Figure 1); and a second internal bus coupled to said processor cores, said memory subsystem, and said DMA-type peripherals (See Figure 1 Number 102), said second internal bus uses an architecture that carries signals from signal initiators to signal targets (See Figure 1); wherein said first internal bus and said second internal bus have an overlapping topology enabling both busses to access a plurality of common devices (See Figure 1), and that each topology is a bussed topology (See Figure 1). Hofmann does not teach that said first internal bus uses an architecture with a latency tolerant signal protocol carries signals from signal initiators to signal targets, wherein said signals are point-to-point and registered signals, and said latency tolerant signal protocol further comprises full handshaking; wherein said architecture with said latency tolerant signal protocol of said first internal bus provides for an arbitrary number of pipeline stages between any signal initiator and any signal target wherein said arbitrary number of pipeline stages are added during the floorplanning of the semiconductor device without requiring a subsequent design or floorplanning iteration, wherein said arbitrary number of pipeline stages comprise one or more of flip-flops, multiplexing routers, or decoding routers; said second internal bus uses said architecture with said latency tolerant signal protocol that carries signals from signal initiators to signal targets; wherein said architecture with said latency tolerant signal protocol of said second internal bus provides for said arbitrary number of pipeline stages between any signal initiator and any signal target wherein said arbitrary number of pipeline stages are added during the floorplanning of the semiconductor device without requiring a subsequent design or floorplanning iteration. AAPA teaches that it is

known in the art to construct the buses of an SOC device using pipeline stages, which provide a latency tolerant signal protocol. AAPA requires no set amount of pipeline stages, and thus, the number of pipeline stages used is arbitrary (See Page 4 Paragraph 8). AAPA further teaches that a common solution in creating a pipeline is to insert a flip-flop in the path to capture and re-launch the signal (See Page 4 Lines 15-18). LaBerge teaches a system controller ASIC, which is equivalent to an SOC (See Figure 1 Number 30) containing programmable circuits, such as the pipeline stages of AAPA (See Figure 1 Number 80 and Column 3 Lines 44-55), that are designed into the chip from the beginning, but are not initially connected to the connection circuitry (See Column 3 Lines 22-33). The programmable circuits of LaBerge can then be selectively connected to the connection circuitry without requiring a fundamental redesign of the chip (See Column 3 Lines 24-28 and 30-43). Sheafor teaches using registered signals on a bus (See Figures 2 and 3 and Column 5 Lines 24-53). Qureshi teaches the use of a point-to-point bus (See Column 1 Lines 16-30). Pawlowski teaches a signaling protocol that uses full handshaking (See Column 1 Lines 19-47).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Hofmann with the use of pipeline segments on a bus of AAPA and the pipeline circuits laid out during floorplanning and capable of being connected to the interconnect bus at a later time, as taught by LaBerge, the registered signals of Sheafor, the point-to-point bus of Qureshi, and the handshaking protocol of Pawlowski, resulting in the invention of Claim 41, in order to enable shorter clock cycles by reducing the distance that must be traversed by a signal

within a single clock cycle (See Page 4 Lines 15-23 of AAPA), to achieve higher operating frequencies and better performance (See Page 4 Lines 13-14 of AAPA); to allow easier modifications of the circuit designs by designing the programmable circuits into the chip from the beginning so that they are available to implement modifications without a fundamental redesign of the chip (See Column 3 Lines 30-35 of LaBerge); because flip-flop interfaces are advantageous and serve to convert the unidirectional buses of the physical layer to a bi-directional bus arrangement (See Column 5 Lines 44-48 and Column 6 Lines 22- 24 of Sheafor); because point-to-point buses have lower latency, minimal bus contention, and the ability to support multiple simultaneous data transfers (See Column 1 Lines 26-28 of Qureshi); and because handshaking allows an asynchronous communication protocol to be used, which provide very high speed transfers of information between I/O devices and host computers and do not rely on a central clock which can limit the bandwidth (See Column 1 Lines 19-28 of Pawlowski).

4. Claims 42 and 43 recite limitations which are substantially equivalent to those of Claim 41 and are rejected under similar reasoning.

5. Claims 41, 42, and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hofmann, US Patent Number 6,594,814 to Jou et al. ("Jou"), LaBerge, Sheafor, Qureshi, and Pawlowski.

6. In reference to Claim 41, Hofmann teaches a system-on-chip (SOC) semiconductor device, comprising one or more processor cores (See Figure 1 'PPC405 CPU'), one or more peripherals (See Figure 1 'I^2C', 'GPIO', and 'UART'), one or more DMA-type peripherals (See Figure 1 'DMA Controller'), and a memory subsystem (See Figure 1 'SDRAM Controller'); a first internal bus coupled to said processor cores and to said peripherals (See Figure 1 Number 101), said first internal bus carrying signals from signal initiators to signal targets (See Figure 1); and a second internal bus coupled to said processor cores, said memory subsystem, and said DMA-type peripherals (See Figure 1 Number 102), said second internal bus uses an architecture that carries signals from signal initiators to signal targets (See Figure 1). Hofmann does not teach that said first internal bus uses an architecture with a latency tolerant signal protocol carries signals from signal initiators to signal targets, wherein said signals are point-to-point and registered signals, and said latency tolerant signal protocol further comprises full handshaking; wherein said architecture with said latency tolerant signal protocol of said first internal bus provides for an arbitrary number of pipeline stages between any signal initiator and any signal target wherein said arbitrary number of pipeline stages are added during the floorplanning of the semiconductor device without requiring a subsequent design or floorplanning iteration, wherein said arbitrary number of pipeline stages comprise one or more of flip-flops, multiplexing routers, or decoding routers; said second internal bus uses said architecture with said latency tolerant signal protocol that carries signals from signal initiators to signal targets; wherein said architecture with said latency tolerant signal protocol of said second internal bus provides for said arbitrary

number of pipeline stages between any signal initiator and any signal target wherein said arbitrary number of pipeline stages are added during the floorplanning of the semiconductor device without requiring a subsequent design or floorplanning iteration. Jou teaches that the use of pipelining is well-known in integrated circuit design (See Abstract), as is the use of pipelines having a dynamically variable number of stages (See Column 1 Lines 55-58 and Column 2 Lines 12-17) comprising flip-flops (See Figure 9 Number 5) and multiplexing routers (See 9 Number 41). LaBerge teaches a system controller ASIC, which is equivalent to an SOC (See Figure 1 Number 30) containing programmable circuits, such as the pipeline stages of AAPA (See Figure 1 Number 80 and Column 3 Lines 44-55), that are designed into the chip from the beginning, but are not initially connected to the connection circuitry (See Column 3 Lines 22-33). The programmable circuits of LaBerge can then be selectively connected to the connection circuitry without requiring a fundamental redesign of the chip (See Column 3 Lines 24-28 and 30-43). Sheafor teaches using registered signals on a bus (See Figures 2 and 3 and Column 5 Lines 24-53). Qureshi teaches the use of a point-to-point bus (See Column 1 Lines 16-30). Pawlowski teaches a signaling protocol that uses full handshaking (See Column 1 Lines 19-47).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Hofmann with the use of pipelines having a dynamically variable number of stages of Jou and the pipeline circuits laid out during floorplanning and capable of being connected to the interconnect bus at a later time, as taught by LaBerge, the registered signals of Sheafor, the point-to-point bus of Qureshi,

and the handshaking protocol of Pawlowski, resulting in the invention of Claim 41, in order to enable shorter clock cycles by reducing the distance that must be traversed by a signal within a single clock cycle (See Page 4 Lines 15-23 of AAPA), because pipelining is a well-known efficient technique for optimally designing high performance digital circuits (See Abstract of Jou), to achieve optimal pipeline speed (See Column 2 Lines 14-17); to allow easier modifications of the circuit designs by designing the programmable circuits into the chip from the beginning so that they are available to implement modifications without a fundamental redesign of the chip (See Column 3 Lines 30-35 of LaBerge); because flip-flop interfaces are advantageous and serve to convert the unidirectional buses of the physical layer to a bi-directional bus arrangement (See Column 5 Lines 44-48 and Column 6 Lines 22- 24 of Sheafor); because point-to-point buses have lower latency, minimal bus contention, and the ability to support multiple simultaneous data transfers (See Column 1 Lines 26-28 of Qureshi); and because handshaking allows an asynchronous communication protocol to be used, which provide very high speed transfers of information between I/O devices and host computers and do not rely on a central clock which can limit the bandwidth (See Column 1 Lines 19-28 of Pawlowski).

7. Claims 42 and 43 recite limitations which are substantially equivalent to those of Claim 41 and are rejected under similar reasoning.

Response to Arguments

8. Applicant's arguments filed 7 January and 5 April 2006 have been fully considered but they are not persuasive.

9. Applicant has argued the Examiner's determination regarding Applicant Admitted Prior Art, specifically that "the Examiner's argument is that the claimed invention and the solution solved by the claimed invention render the claimed invention either anticipated or obvious in view of its own disclosure." (See Page 9 Section 5). In response, the Examiner notes that, as shown in the above rejections, the only portion of the disclosure relied upon as being admitted prior art is Paragraph 8 of Page 4, which is part of the "Description Of The Related Art" (See Page 3 Line 9) and which states, among other things, that "The common solution to the problem of extended signal propagation times caused by the physical interconnect is pipelining..." (See Page 4 Paragraph 8). Thus, what is being relied upon as prior art is what was disclosed as being a common solution.

10. Applicant has argued that the elements identified in the paragraph spanning Pages 10 and 11 of Section 6 were not found by the Examiner in either Hofmann or LaBerge, and were only cited as being found or taught in Applicant's disclosure. In response, the Examiner notes that Applicant Admitted Prior Art was not relied upon to teach all of the identified elements. Rather, Applicant Admitted Prior Art was relied

upon to teach that it is known in the art to construct the buses of an SOC device using pipeline stages, which provide a latency tolerant signal protocol (See Page 4 Lines 15-18). AAPA requires no set amount of pipeline stages, and thus, the number of pipeline stages used is arbitrary (See Page 4 Paragraph 8). LaBerge was relied upon to teach the remaining elements not taught by Hofmann. One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

11. Applicant has argued that the elements identified in the third paragraph of Page 12 of Section 7 were not found by the Examiner in Hofmann, LaBerge, or Jou and were only cited as being found or taught in Applicant's disclosure. Specifically, the Applicant has argued that "The only reference that the Examiner cites in a back door fashion where these elements are found or taught is the Applicant's own disclosure." (See Page 12 Paragraph 5) and "The Examiner actually has to reference his determination of AAPA to show the above elements that he admits that Hofmann does not disclose or teach." (See Page 13 Paragraph 2). In response, the Examiner notes that, as shown above, no portion of this rejection makes any reference to AAPA. Contrary to Applicant's argument that "Jou neither adds to or subtracts from the Examiner's use of Hofmann or LaBerge", the Examiner notes that Jou is relied upon to teach that the use of pipelining is well known. Applicant is requested to identify where in the rejection

AAPA was relied upon in a back door or backhanded fashion to teach any of the limitations.

12. Applicant has argued that the cited references do not teach all of the claim elements and limitations (See Page 14 Paragraph 3). In response, the Examiner notes that, as shown in the above rejections, the Claim limitations (as amended) are taught by either the combination of Hofmann, AAPA, LaBerge, Sheafor, Qureshi, and Pawlowski, or the combination of Hofmann, Jou, LaBerge, Sheafor, Qureshi, and Pawlowski.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The Examiner can normally be reached on Monday-Thursday (7-3), Alt. Fridays (7-2).

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TJC

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